ABSTRACT OF THE DISCLOSURE

CIRCUIT AND METHODS TO IMPROVE THE OPERATION OF SOI DEVICES

According to the present invention, a circuit and methods for enhancing the operation of SOI fabricated devices are disclosed. In a preferred embodiment of the present invention, a pulse discharge circuit is provided. Here, a circuit is designed to provide a pulse that will discharge the accumulated electrical charge on the body of the SOI devices in the memory subarray just prior to the first access cycle. As explained above, once the accumulated charge has been dissipated, the speed penalty for successive accesses to the memory subarray is eliminated or greatly reduced. With a proper control signal, timing and sizing, this can be a very effective method to solve the problem associated with the SOI loading effect. Alternatively, instead of connecting the bodies of all SOI devices in a memory circuit to ground, the bodies of the N-channel FET pull-down devices of the local word line drivers can be selectively connected to a reference ground. This would enable the circuit to retain most of the speed advantages associated with SOI devices while overcoming the loading problem described above. With this preferred embodiment of the present invention, the major delay caused by the bipolar loading effect is minimized while the speed advantage due to providing a lower, variable Vt effect is preserved. The overall body resistance of the individual devices has a minimal effect on the device body potential.